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Implementation of an 8-bit Low-power Multiplier based on Reversible Gate Technology

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***Abstract*— Reversible logic has attracted tremendous interest among the researchers in low power VLSI field due to their simple structure and improved energy efficiency. In this paper, the implementation of an 8-bit low power multiplier based on reversible gate technology is reported. The structure of the reversible gate multiplier consists of following components: the first part is the reversible partial product generator circuit (PPGC) which will be realized by reversible AND gate; the second part is constructed by several TSG gates whose function is to add the carryout of the previous level and PPCG of current level together. In the second part, some XNOR gates and NOR gates with improved designs to save power and speed up the performance are presented. The 8-bit reversible gate multiplier is designed and simulated in PSPICE. PSPICE simulation verifies the correct function of the multiplier. In order for comparison, an 8-bit static CMOS multiplier is also designed. PSPICE power simulation is used to simulate the power consumption of both reversible gate multiplier and the static CMOS multiplier for the same given input pattern sequence. Simulation results show that reversible gate multiplier leads to effective power saving compared to static CMOS multiplier.**

Keywords*— Reversible logic, Reversible gate, Low power VLSI, Low power CMOS design.

I. INTRODUCTION

Reversible Logic is being developed rapidly in the recent years because of the power dissipation can be reduced by their own abilities in low power VLSI design. It has been widely used in many fields such as Low Power CMOS design, quantum computing, DNA technology[1], cryptography and nanotechnology[2,3]. The definition of Reversible Logic is: in a reversible circuit (gate), the number of inputs is as same as the number of outputs, the vectors of inputs and outputs have the logic function of one-to-one mapping; thus the vector of input states can be always reconstructed from the vector of output states[4-6].

The advantages of reversible gates have two aspects: the first is that they do not erase (lose) information; the second is that they dissipate very less heat[7]. Therefore, these circuits can generate unique output vector from each input vector, there is a one-to-one mapping between input and output vectors. R.Landauer[8] has shown that for irreversible logic computations, each bit of information lost generateskTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [5]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [9], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation.

II. 8×8 Reversible Multiplier Based on TSG Gate design

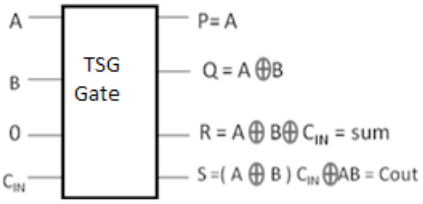

Fig.1: TSG Gate working as reversible full adder

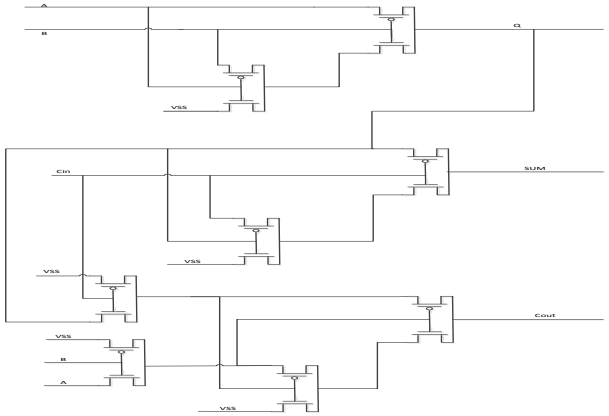

Fig.2: TSG Gate transistor realization

The reason to choose TSG Gate: among the five types of reversible gates, apparently the TSG gate can be revised into a

full adder which is the fundamental component to construct a multiplier most easily. Because the proposed TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder [10].

We use P-spice Power Simulation to simulate the circuit above, and get a nearly correct function. In the simulation result, we found Signal Degradation Problem exist in the full adder circuit. The Signal Degradation Problem is defined as the loss of quality of an electronic signal, because the character of NMOS and PMOS. To be specific, PMOS degrades 0 and NMOS degrades 1, which means when the signal 1 as the voltage 5V goes through NMOS, it would not be 1, it would be a little bit lower than 1 as 4.3V; In the same way, when signal 0 as voltage 0V goes through the PMOS, it would be a little higher than 0 as 0.7V. Admittedly, the 0.7V difference is not significant in a simple full adder circuits. But when hundreds of these transistors integrate together, there will be hundreds of 0.7V lost which will change the circuits function completely. Conclusively, for keep the multiplier function correctly, we must find a way to resolve the Signal Degradation Problem.

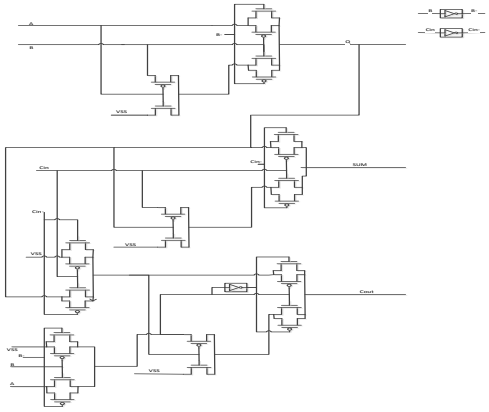

Fig.3: Transient reversible logic(TRL)full adder

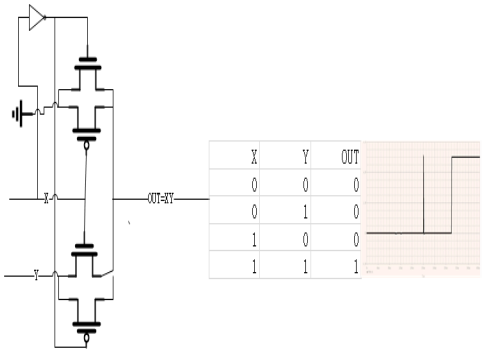

Fig.4: TRL And Gate

From the Fig. above, we can get the correct simulation result which is what we want this time. The reason we can get the correct result is that in the circuit above, the signal 1 which supposed to go through NMOS will bypass it and though the PMOS which is right above the NMOS and has the common source and drain with the NMOS. In the same way, the signal 0 which supposed to go through PMOS will bypass it and through the NMOS which is right above the PMOS and has the common source and drain with the PMOS. So consequently the signal 1 always goes through PMOS, while the signal 0 always goes through NMOS. In this way, we can avoid the signal degradation problem, but will add more transistors and reduce the efficiency of the circuits. We will get specifically how much we reduce the efficiency based on the analysis in the aspects of delay time and power consumption of the whole 8-bit reversible gate multiplier circuit. And we can use this kind of logic on many other reversible gates as Reversible XOR Gate or the whole TSG gate, and we name the new logic to avoid the signal degradation as Transient Reversible Logic (TRL).

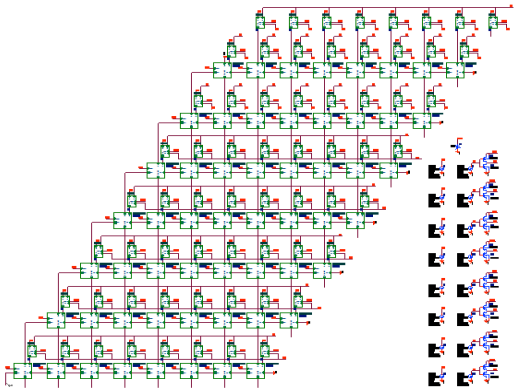

Fig.5: TRL 8×8 multiplier

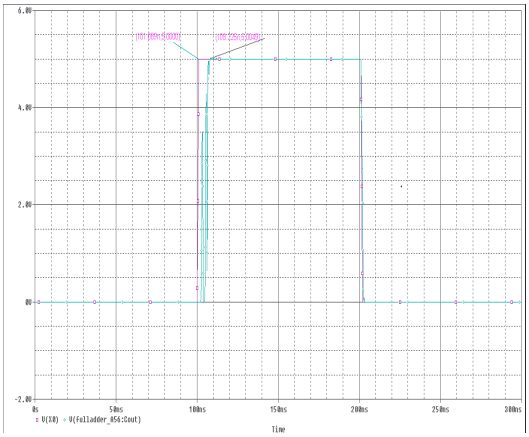

Fig.6: Time delay of TRL 8×8 multiplier

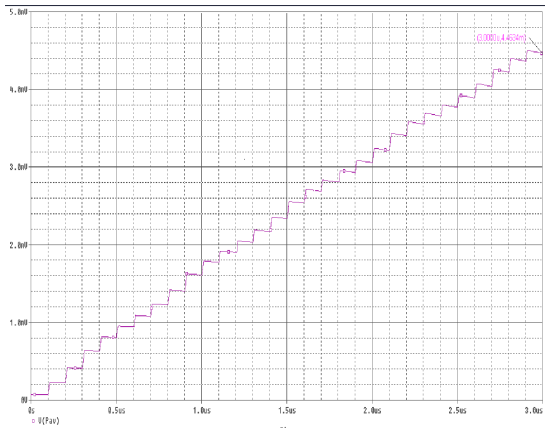

Fig.7: Power Simulation of TRL 8×8 Multiplier

The Fig.4 shows the hierarchical design of the TRL 8×8 Multiplier, in this design we use  to present AND gate and  to present Full Adder. From the figures above, we can get the Time Delay and Power Consumption by P-spice. We will use these data to compare them with CMOS 8×8 Multiplier as next chapter.

III. CMOS 8×8 Multiplier Design

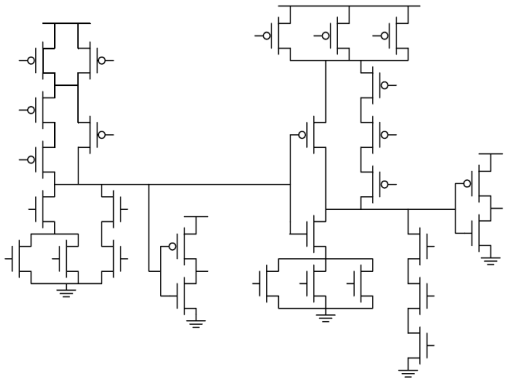

Fig.8 Transistor realization of CMOS full adder

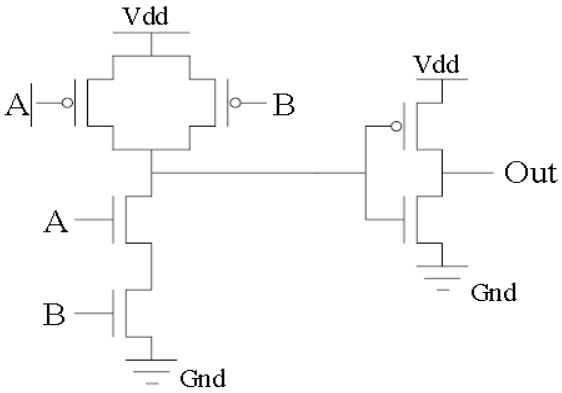

Fig.9: CMOS And Gate

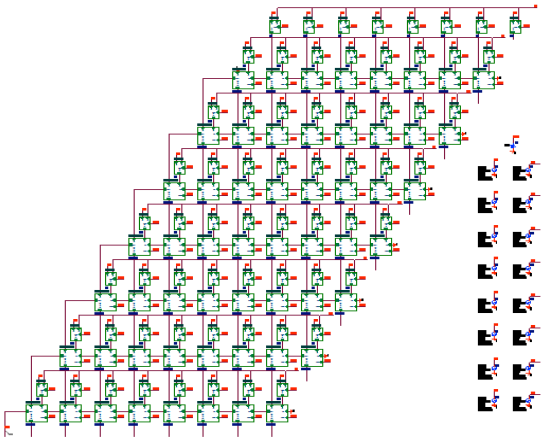

Fig.10: CMOS 8×8 multiplier

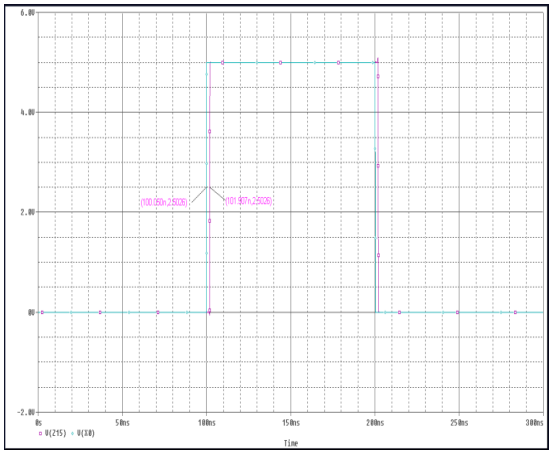

Fig.11: Delay time of CMOS 8×8 multiplier

From the Fig above, we can know thar the time difference between Z15 and X0 is 1.875ns which also presents the delay time of CMOS Multiplier.

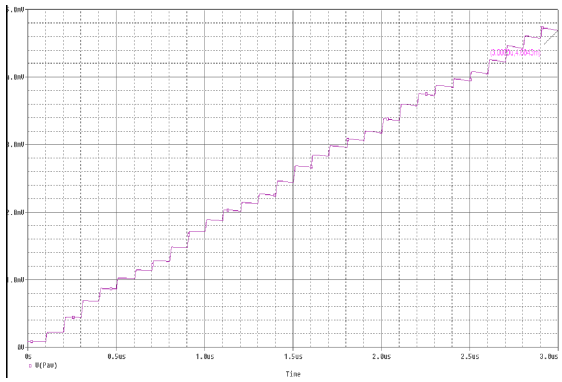

Fig.12: Power consumption of CMOS 8×8 multiplier

The auxiliary part of CMOS.cir is exactly same as TRL.cir, which means the two circuits of CMOS 8×8 Multiplier and TRL 8×8 Multiplier have the same input pattern, model, transistor size and VDD voltage. From the Fig above, we can get the CMOS Multiplier consumes 4.6843mw at 3us of the running period 3.0us.

Through some simple calculation, we can derive that TRL 8×8 Multiplier can save 4.7% power consumption, but sacrifice 280% Delay Time and 5.7% number of transistors more than CMOS 8×8 Multiplier uses. In another word, the low speed and too large transistor number restrict the TRL 8×8 Multiplier application in our real life. So from analysis above, we can get that the TRL Multiplier has its advantage on Power Consumption, but sacrifices too much delay time. So in order to improve TRL, we combine two circuits TRL AND gate and CMOS Full Adder together in next chapter.

IV. TRL&CMOS 8×8 Multiplier

We follow Fig.4 hierarchical circuit. This time we use the circuit in Fig.3 to present the AND gate  , and we use Fig.7 to present the Full Adder  . We also get the delay time and power consumption as following:

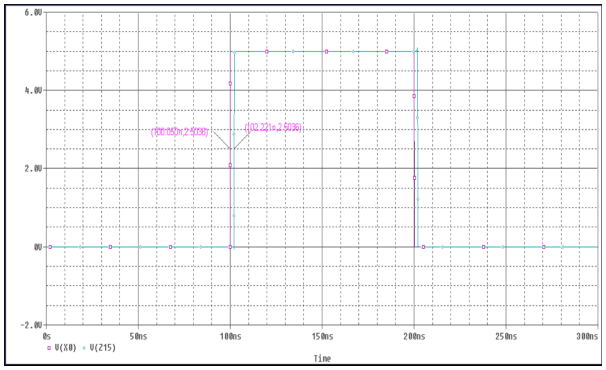

Fig.13: Delay time of CMOS&TRL 8×8 multiplier

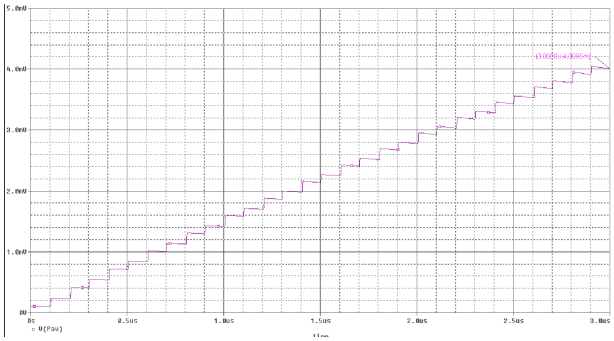

Fig.14: Power consumption of CMOS&TRL 8×8 multiplier

From the Fig. 13 and Fig. 14, we can get that the delay time of CMOS&TRL Multiplier is 2.171ns and the power consumption of CMOS&TRL Multiplier is 4mw. The transistor number of CMOS&TRL 8×8 Multiplier is . When we put the three Multipliers (CMOS Multiplier, TRL Multiplier and CMOS&TRL Multiplier) together, we can realize the practical applicability of CMOS&TRL Multiplier.

V. Results and Discussions

Table1:Comparison of Three Different Kinds' Multiplier

	TRL 8×8 Multiplier	CMOS 8×8 Multiplier	CMOS&TRL 8×8 Multiplier
Delay Time	7.136ns	1.875ns	2.171ns
Power Consumption	4.4634mW	4.6843mW	4mW
Number of Transistors	2064	1952	1840

In the aspect of speed, power consumption and number of transistors, the CMOS&TRL Multiplier has its own advantages. Specifically, compared with the most traditional and widely used multiplier- CMOS Multiplier, the CMOS&TRL Multiplier is 13.5% slower, but consumes 14.6% less energy, and save 5.7% transistors of COS Multiplier. Consequently, the CMOS&TRL Multiplier can be used in the field of low-power aspect very widely, because the CMOS&TRL Multiplier can save a lot of energy and works in a smaller chip. In the future, we may use the TRL Tech to optimize ALU (Arithmetic and Logic Unit) circuit just as what we did on the multiplier.

VI. Conclusions and Future Work

We would further reduce the overhead of the reversible gate logic, so that the power saving of reversible gate multiplier can be even more. In this work, the simulation results show that the reversible gate multiplier saves about 14% of power compared to static CMOS design. Compared to static CMOS multiplier, the reversible gate multiplier needs

circuit blocks to avoid the signal degradation due to pass transistor logic. This adds extra power to the reversible gate logic and reduce its overall power saving. In the future, we will focus our research on how to reduce this overhead, so that the power saving of reversible gate multiplier can be even more significant compared to the static CMOS design. The proposed reversible gate design will be extended to other VLSI circuits such as low power CMOS design, quantum computing, optical computing, digital signal processing(DSP), computer graphics.

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